# Project 3A

## Objective

The goal of this subset of Project 3 is to create and reuse modules, from previous projects and homework, in order to implement a comparator system and test its functionality. This system will be used to explore the DE1-SoC board and the set up within Quartus. This aspect of the project is limited by the absence of a physical board.

This project allowed for students to explore the implementation of our own modules to a physical device. Having both the pin assignments and synthesizable design in mind allowed for a progression of thought for digital design. The end vision of this class is now in sight as we learn to apply fundamental concepts to large applications.

## Design

The design of the comparator is like the design of Project 2. This system uses the hc85 module as well as two different drivers for a seven-segment display. The top-level module requires a simple connecting of wires. The switches on the DE1-SoC board are used for the two 4-bit inputs to the comparator. The output of the comparator is fed into one the seven-segment display drivers that displays either a g, an E, or an L. This driver is detailed in the following paragraph. To complete the top-level module, the two 4-bit inputs from the switches are also connected to two seven-segment drivers. All three display drivers are connected to the displays on the DE1-SoC board.

The seven-segment display driver connected to the output of the comparator is a modified module based of the hexadecimal display driver. This new driver uses the same procedural model, but instead of taking a 4-bit hexadecimal input it takes three inputs – the outputs of the comparator. Based on which input is active high, the display will output a 7-bit binary value to display a g, an E, or an E for greater than, equal to, or less than respectively.

## Testing

In order to test the comparator system, several test cases were used. Within each test case the switches of the DE1-SoC board, the SW input, were varied in order to simulate an adequate amount of outputs from the system. Within the testbench and each individual test case the expected output is included. The first nine cases test the three different outputs from the system – less than, equal, and greater than. The last case tests the correct switching between outputs. Included below is the waveform from the testbench simulation.

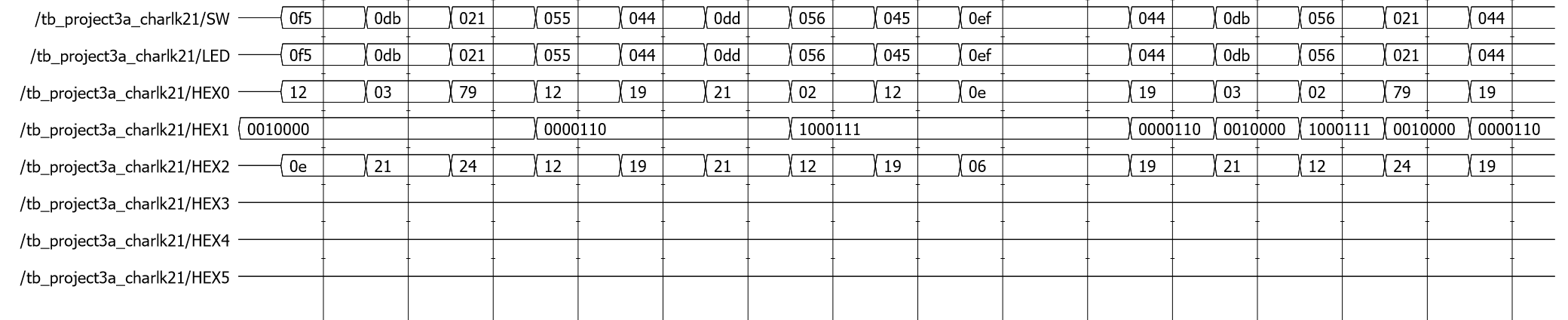


Figure 1. Comparator System Simulation Waveform